AF

TRANSMITTAL LETTER (General - Patent Pending)	Docket No. GB-000068

In Re Application Of: **Octavius J. Morris et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
09/855,115	14 MAY 2001	Behrooz M. SENFI	20987	2613	8730

Title: **VIDEO SIGNAL ENCODING AND BUFFER MANAGEMENT**

COMMISSIONER FOR PATENTS:

Transmitted herewith is:

Reply Brief

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Dated: **24 March 2006**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	09/855,115
Applicants	:	Octavius H. MORRIS et al.
Filed	:	14 May 2001
TC/A.U.	:	2613
Examiner	:	Behrooz M. SENFI
Atty. Docket	:	GB-000068

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REPLY BRIEF

U.S. Patent and Trademark Office
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Sir:

In response to the Examiner's Answer dated 26 January 2005, finally rejecting pending claims 1-14, and in support of the Notice of Appeal filed on 25 May 2005, Applicants hereby submit this Reply Brief.

Arguments Not Addressed At All by Examiner's Answer

Surprisingly, the Examiner's Answer fails completely to address several points made in Applicant's Reply Brief.

1. The Examiner Has Still Not Cited Anything As Even Allegedly Corresponding to the Source of Encoded Digital Video Images of Claim 10

M.P.E.P. § 2131 provides that:

> "TO ANTICIPATE A CLAIM, THE REFERENCE MUST TEACH EVERY ELEMENT OF THE CLAIM "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Among other things, the digital video processing means of claim 10 includes a source of encoded digital video images coupled with a decoder for the encoded images.

Throughout the prosecution of this application, the Examiner has never once cited anything in any cited prior art reference as disclosing or corresponding to the recited source of encoded digital video images. Applicants have already pointed out this deficiency in the response to previous Office Actions, and in the Appeal Brief. The Examiner has not responded.

So, Applicants respectfully submit that, very clearly, the rejection of claim 10 cannot be maintained.

2. The Examiner Has Never Yet Provided Any Motivation for the Proposed Combination of Dieterich and Kato with Respect to Claim 5

M.P.E.P. § 2143.01 provides that:

> "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art."

See also In re Lee, 277 F.3d 1338, 1342-44, 61 USPQ2d 1430, 1433-34 (Fed. Cir. 2002) (In reversing the Board's decision, the court stated "'common knowledge

and common sense' on which the Board relied in rejecting Lee's application are not the specialized knowledge and expertise contemplated by the Administrative Procedure Act. Conclusory statements such as those here provided do not fulfill the agency's obligation....The board cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims, but must set forth the rationale on which it relies.")

Here, the Examiner has failed to cite any teaching, suggestion, or motivation in the prior art for modifying Dieterich to make each slice comprise sixteen luminance lines (claim 5) by combining Dieterich with Kato. Applicants have already traversed this combination in the response to previous Office Actions, and in the Appeal Brief. Yet the Examiner does not address this traversal at all in the Examiner's Answer.

Accordingly, Applicants respectfully submit that the Examiner's rejection of claim 5 cannot be maintained.

Response to New Arguments and Citations in Examiner's Answer

The method of claim 1 includes reading encoded field data into the buffer, and subsequently reading the stored data out of the buffer at a bit rate determined at least partially by the fullness of the buffer. Meanwhile the apparatus of claim 6 includes a buffer coupled to receive encoded field data from the encoding stage and arranged to subsequently output the stored data at a bit rate determined at least partially by the fullness of the buffer

In the Examiner's answer, for the first time, the Examiner states that Dieterich discloses the feature of reading the stored (i.e., encoded) data out of the buffer at a bit rate determined at least partially by the fullness of the buffer in "the arrows going in and out from the buffer" in FIGs. 6 and 7 "which indicates data being read in and read out from the buffer and being controlled by the rate controller 630 and 710 to prevent overflow and/or underflow with respect to the size of the buffer." The Examiner also cites col. 3, lines 40-45 and col. 6, lines 16-31 and 43-45.

Applicants respectfully submit that none of the text or figures cited by the Examiner here for the first time discloses or remotely suggests reading the stored data out of the buffer at a bit rate determined at least partially by the fullness of the

buffer.

First, here is the cited text at col. 3, lines 40-45:

> the image sequence on path **175** that is being delayed. As such, the delay section **170** can be implemented using a temporary storage device, e.g., a First-In-First-Out (FIFO) buffer of sufficient size to hold a portion of the image sequence. The size of the buffer is dictated by the requirements of a particular application. It should be noted that the

It is apparent that the text at col. 3, lines 40-45 does **not** disclose or suggest reading the stored data out of the buffer at a bit rate determined at least partially by the fullness of the buffer. Indeed, the text does not even pertain to the encoder 180, or the encoder embodiments of FIGs. 6 and 7 including Buffers 190 and 214, at all, but instead is merely discussing a FIFO used as delay element 170 for image source material that has not even been encoded yet!!! So it is ridiculous to suggest that anything in col. 3, lines 40-45 discloses reading the stored **encoded** data out of a buffer at a bit rate determined at least partially by the fullness of the buffer.

Next, here is the cited text at col. 6, lines 16-31 and 43-45:

> The data stream is received into a "First In-First Out" (FIFO) buffer **690**, which is used to match the encoder output to the channel for smoothing the bit rate. Thus, the output signal of FIFO buffer **690** on path **695** is a compressed representation of the input video image on path **610** (or a compressed difference signal between the input image and a predicted image), where it is sent to a storage medium or telecommunication channel via path **695**.
>
> The rate control module **630** serves to monitor and adjust the bit rate of the data stream entering the FIFO buffer **690** to prevent overflow and underflow on the decoder side (within a receiver or target storage device, not shown) after transmission of the data stream. Thus, it is the task of the rate control module **630** to monitor the status of buffer **690** to control the number of bits generated by the encoder.

> To illustrate, the side information in the format of raw data, e.g., bit rates corresponding to the use of the quantization scales of 15 and 10, as discussed above, can be used by the rate control module **630** to determine whether the buffer fullness is at a state that will allow the use of a finer quantization scale. Alternatively, the rate control module **630** may simply accept and apply the recommended quantization scale from the side information for the current frame.

Again, the cited text does not disclose or remotely suggest reading the stored data out of the buffer at a bit rate determined at least partially by the fullness of the buffer. Instead, and in direct contrast, the text teaches that:

> "The rate control module 630 serves to monitor and adjust the bit rate of the data stream **entering** the FIFO buffer 690 to prevent overflow and underflow **on the decoder side** (**within a receiver or target storage device, not shown**) after transmission of the data stream"

(emphasis added).

So, in direct contrast to rate control module 690 **read**ing data **out of the buffer** at a bit rate determined at least partially by the **fullness of the buffer**, instead rate control module 690 **writes** data **into the buffer** at a bit rate such that a completely different buffer in a **target receiver** will not overflow or underflow!

And finally, of course this disclosure is entirely consistent with what is shown in FIGs. 6 and 7 which show Rate Control 630 and Rate Controller 710 each controlling the rate at which a coder **writes data** into Buffers 690 and 714, respectively. In that regard, it is instructive that in FIGs. 6 and 7 there are no arrows going **from** Rate Control 630 and Rate Controller 714 **to** Buffers 690 and 714, respectively, that might control any operation of the Buffers.

Accordingly, for at least these reasons, once again Applicants respectfully submit that claims 1 and 6 are clearly patentable over Dieterich.

Furthermore, as explained earlier, in the method of claim 1, the encoded data for the slice is read into the encoder buffer and subsequently read out therefrom on completion of encoding of the slice.

The Examiner States that Dieterich discloses that "a bit budget management optimizes coding efficiency with controlling overflow and underflow conditions, which is actually based on the data/slice being read-in and read out from the buffer with respect to the completion state citing col. 14, lines 21-46. Here is the text at col. 14, lines 21-46:

> Some encoders provide bit budget control beyond the frame level, i.e., there are bit budgets for a stripe, a row, or a slice of an image (a stripe may be multiple rows, and a slice is either the same as or a fraction of the length of a row). Accurate bit budget management optimizes coding efficiency while controlling overflow and underflow conditions.
>
> Thus, it would be very advantageous to be able to extract side information that is indicative of bit budget selections for the entire image sequence or portions thereof in advance. The extraction of such bit budget selections side information can be achieved by using an encoder **910** having coding parameter settings that are similar to the encoder **180**. Namely, an image sequence is initially encoded using the encoder **910** in the pre-processing section **110**. This allows the encoder **910** to verify the bit budgeting methods of encoder **180** in advance. Alternatively, one or more encoders **910** in the pre-processing section **110** can be employed to analyze a plurality of bit budgeting methods.
>
> The result from the above analysis by the encoder(s) **910** can be represented as side information in the format of raw data (the number of actual bits used to encode a stripe, a row, or a slice of a particular frame) or as a recommendation to use a particular bit budget for a stripe, a row, or a slice for a particular frame or a choice of bit budgeting method. Bits Needed to Encode This frame at a Constant Quantization Scale/Quality

Once again, it is apparent that the text at col. 14, lines 21-46 does **not** disclose or suggest that encoded data for the slice is read into the encoder buffer and subsequently read out therefrom on completion of encoding of the slice. Indeed, the text does not even pertain to the encoder 180 or the encoder embodiments of FIGs. 6 and 7 include buffers 690 and 714 at all, but instead merely discusses an embodiment of side information inserter 160.

Accordingly, for at least these additional reasons, once again Applicants respectfully submit that claims 1 and 6 are clearly patentable over Dieterich. Claims 2-5 and 7-14 dependent therefrom are deemed similarly patentable.

Conclusion

For all of the foregoing reasons, Applicants respectfully submits that claims 1-14 are all patentable over the cited prior art. Therefore, Applicants respectfully request that claims 1-14 be allowed and the application be passed to issue.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future filings to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16, 37 C.F.R. § 1.17, or 37 C.F.R. § 41.20, particularly extension of time fees.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.

Date: 24 March 2006

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